



# **SMPW Service General Description**

**MPW Workshop - ESTEC**

**June 17th, 2004**





## **Space Multi Project Wafer**

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**In our 20 years continuing commitment to give customers access to advanced technologies for Space Applications,**

**Atmel is offering a new Space foundry service:**

**SMPW**

**(Space Multi Project Wafer)**

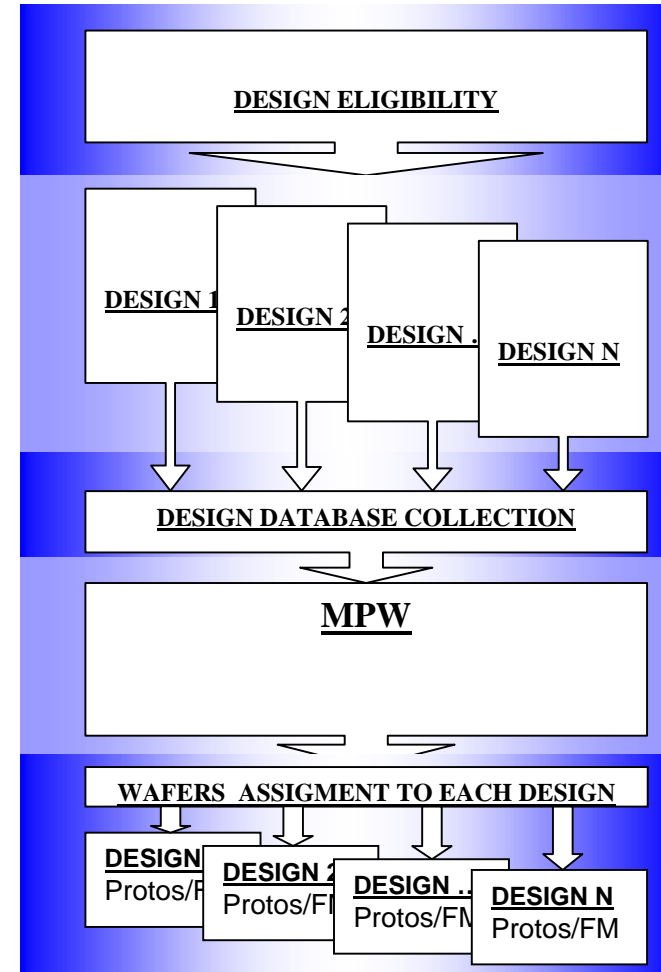
## **SMPW Foundry Service Objectives**

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- **A service for ANY European Space Customer**
  - **On the advanced 0.18 $\mu$ m RHA technology**
  - **With the ATC18RHA ASIC standard cell libraries**
  
- **Reduced manufacturing non recurring costs of ASIC development**
  - **By sharing reticules and silicon costs between several designs**
  
- **Same set of reticules for Prototyping and Flight Models**
  
- **In case of run overbooking, ESA will apply following priority criteria**
  - **1 ESA mission ASICs**
  - **2 ESA R&D ASICs**
  - **3 non ESA commercial ASICs**
  - **4 non ESA R&D ASICs**

## Generalities (1)

- **No design constraints specific to SMPW**
  - ATC18RHA design kit applies without restrictions
  - Each design is developed independently of the others
  - But new synchronization milestones are created
  
- **SMPW is a Space foundry service**
  - The SMPW is limited to reticules and wafers manufacturing
  - 1 sole reticules set for all the designs embarked
  - Several designs manufactured on the same wafer
  - Wafers split in sub-lots assigned to 1 design



## Generalities (2)

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- **SMPW runs will be launched at fix dates made public in advance to the space community**
- **Each run includes**
  - Reticules manufacturing
  - 1 lot with priority for prototyping
- **Complementary lots for Flight Models can be launched**
  - With the same reticules
  - Without date restriction
  - When needs appear
- **ESA reserved and funded 4 runs dedicated to ESA projects**
  - Nevertheless, if surface available on the reticule, non ESA projects could embark on an ESA dedicated run,
    - after ESA approval

## **Generalities (3)**

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- **2 majors milestones dedicated to SMPW management are created**
  - **Logic Review Closing Date (LRCD)**
    - **Fix date**
    - **Firm approval from ESA to what designs are on the run**
    - **Firm confirmation from Atmel to embark the design**
    - **Firm confirmation from customer to embark and meet the schedule of the SMPW**
    - **From this date, cancellation charges apply**
  - **Design Review Closing Date (DRCD)**
    - **Fix date**
    - **Start of the foundry manufacturing**



## **Wafers assignment**

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- **Prototyping**
  - The first lot of 25 wafers will produce in priority prototypes
- **Flight Models**
  - Can be manufactured with the remaining wafers of the first lot (if any)
  - If not, launch of a new lot with the same reticule



## **SMPW Definition and Validation**

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- **Definition and Validation of the SMPW in the frame of an ESA contract**
  - **Atmel led an engineering activity to adapt the existing mono project procedures to the SMPW**
  - **Objectives and constraints**
    - **Reduce customers' foundry costs**
    - **No negative impact from one customer design on the others**
    - **Secure the space quality**
    - **Processes have to be as close as possible of the current space manufacturing flow**
    - **Produce the maximum quantity of parts despite the limitations of equipments**



## **SMPW Definition and Validation**

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- **Technical constraints are impacting mostly the organization of the designs on the reticule**
- **No technical modifications in the process of the wafer**
- **But, the spare areas between the designs will be filled with “dummy structures”**
- **No technical modifications in the probe and assembly processes**
- **But, management rules have been added allowing to treat each wafer sub lot as a mono-project wafer**



## **SMPW Definition and Validation**

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- **Verification with a so-called “Validation Run”**
  - **Reticule using SMPW organization rules**
  - **Production of an engineering wafers lot (prototypes)**
  - **Verification of the complementary management rules introduced in probe and assembly areas**



## **SMPW Definition and Validation**

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- **Designs embarked on the “Validation Run”**
  - **4 designs on 3 different matrix sizes**
    - **1 design on the largest matrix (170 mm<sup>2</sup>)**
    - **1 design on the second largest matrix (114 mm<sup>2</sup>)**
    - **2 designs on the intermediate matrix (74mm<sup>2</sup>)**
- **“Validation Run” schedule**
  - **Design Review Closing Date (DRCD) Mid July 2004**
  - **Prototype assy and test November 2004**
  - **Final Validation Run conclusions December 2004**



## SMPW more information

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- Atmel website ([www.atmel.com](http://www.atmel.com)) will indicate
  - The MPW runs dates
  - The free remaining area on the reticule per run
- Direct link  
[http://www.atmel.com/product/product\\_card.asp?part\\_id=2318](http://www.atmel.com/product/product_card.asp?part_id=2318)
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